Application Report
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TRF6900/MSP430 EVK

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ABSTRACT

This document describes the Texas Instruments (TI) TRF6900/MSP430 evaluation kit (EVK) and associated software, which allows the evaluation and demonstration of the TRF6900, a 900 MHz ISM band transceiver. The supplied evaluation module (EVM) is tailored to operate within the European 868 MHz to 870 MHz band.

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1 Product Support

The TI advantage extends beyond RF to every other major wireless system block.

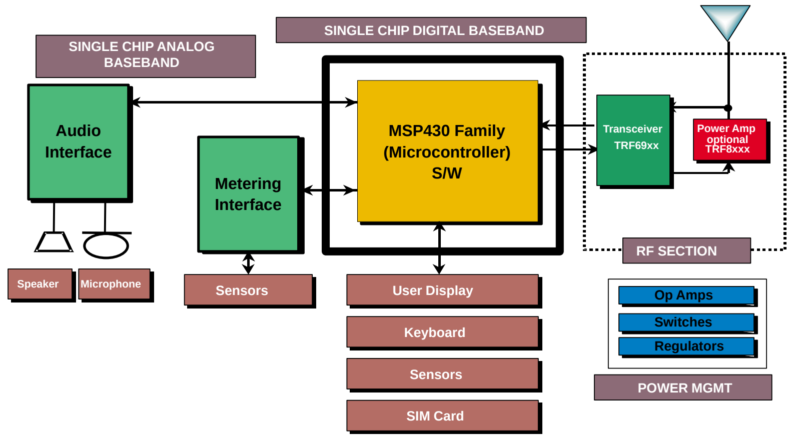


Figure 1. TRF6900/MSP430 System Block Diagram

1.1 Digital Baseband

TI's single-chip digital baseband microcontroller MSP430 was designed specifically for low-power embedded systems.

The customizable platform helps wireless digital ISM band manufacturers to lower component counts, save board space, reduce power consumption, and introduce new features. The enclosed MSP430 software can be used as a starting platform for development to save development costs and achieve faster time to market. At the same time it gives them flexibility and performance to support any ISM standard worldwide.

1.2 Analog Baseband

TI analog baseband components provide a mixed-signal bridge between the real world of analog signals and digital signal processors, the key enabling technology of the digital wireless industry. Using a seamless architecture for wireless communications technology, TI matches its baseband interfaces, radio frequency ICs, and power management ICs to digital signal processing engines to create complete DSP solutions for digital wireless systems.

1.3 Power Management

TI provides power management solutions with integration levels designed to meet the needs of a range of wireless applications. From discrete LDOs and voltage supervisors to complete power supplies for the baseband section, TI power management solutions play an important role in increasing wireless battery life, time-to-market, and system functionality.

For more information visit the industrial RF web site at:

http://www.ti.com/sc/msds2963u

or *the MSP430 Homepage*

www.ti.com/sc/docs/products/micro/msp430/msp430.htm

2 Introduction

The TRF6900/MSP430 evaluation board (EVM) is comprised of a four-layer printed-circuit board and all required components to evaluate the TRF6900. The TRF6900 can be programmed via the onboard parallel interface using the included Windows® based programming tool evaluation software. Several SMA connectors as well as the 14 pin header enable direct access to the transceiver to ease the evaluation

Since the TRF6900 is designed for 900 MHz ISM band systems, the evaluation board demonstrates a setup typically used for the recently introduced European 868 MHz to 870 MHz band. Therefore, the transceiver is optimized to operate between 850 MHz and 890 MHz. The receiver uses low-band injection for a single down conversion to 10.7 MHz.

The onboard MSP430x112 is used in conjunction with the TRF6900 to demonstrate a complete ISM band solution. The included Windows-based system demo software can be used to set up a serial RF link.

The following information is included to aid in the assessment of this device:

- Block diagram and functional description
- Schematic
- Parts list
- PCB layout
- EVM programming tool description
- TRF6900/MSP430 system mode description

3 Warning

The evaluation board can cause interference; in this case, the operator is required to execute appropriate protective measures. The EVK TRF6900 board should only be put into operation by technically qualified personnel and in accordance with the electromagnetic compatibility requirements contained in directive 89/336/EWG.

In accordance with the German Electromagnetic Compatibility Act of 18 September 1998 and the respective legislation in other European countries, appropriate measures have to be taken to avoid electromagnetic disturbance of third parties, including avoidance of disturbances in connection with the radiation or sending of utilizable frequencies.

To avoid disturbances of third parties:

- Maximum input power at LNA_IN should not exceed 0 dBm.
- Utilizable transmit and receive frequencies should be within the European 868 – 870 MHz band.
- The EVK TRF6900 may not be used for radio transmission.

The board was not examined for noise immunity. Any type of electromagnetic disturbance can lead to unexpected operating conditions.

3.1 Means of Conformity

The product conforms to the 89/336/EEC EMC standards relating to electromagnetic compatibility, implemented in Germany by the Electromagnetic Compatibility Act of 18 September 1998 (EMVG, §4.2). This certificate does not contain any statements pertaining to the EMC protection requirements pursuant to other laws, which serve to implement EC directives other than the aforementioned council directive.

4 TRF6900 Functional Description

The TRF6900 is a single-chip transceiver for the new 868 MHz to 870 MHz European band and the North American 915 MHz ISM band. It comprises all active components used to establish a frequency-agile, half-duplex, bidirectional RF link using FM/FSK modulation. The single-chip transceiver operates down to 2.2 V and is especially designed for low power consumption. The integrated direct digital synthesizer (DDS) as used on the EVM board has a channel spacing of approximetely 230 Hz to allow narrow-band and wide-band applications.

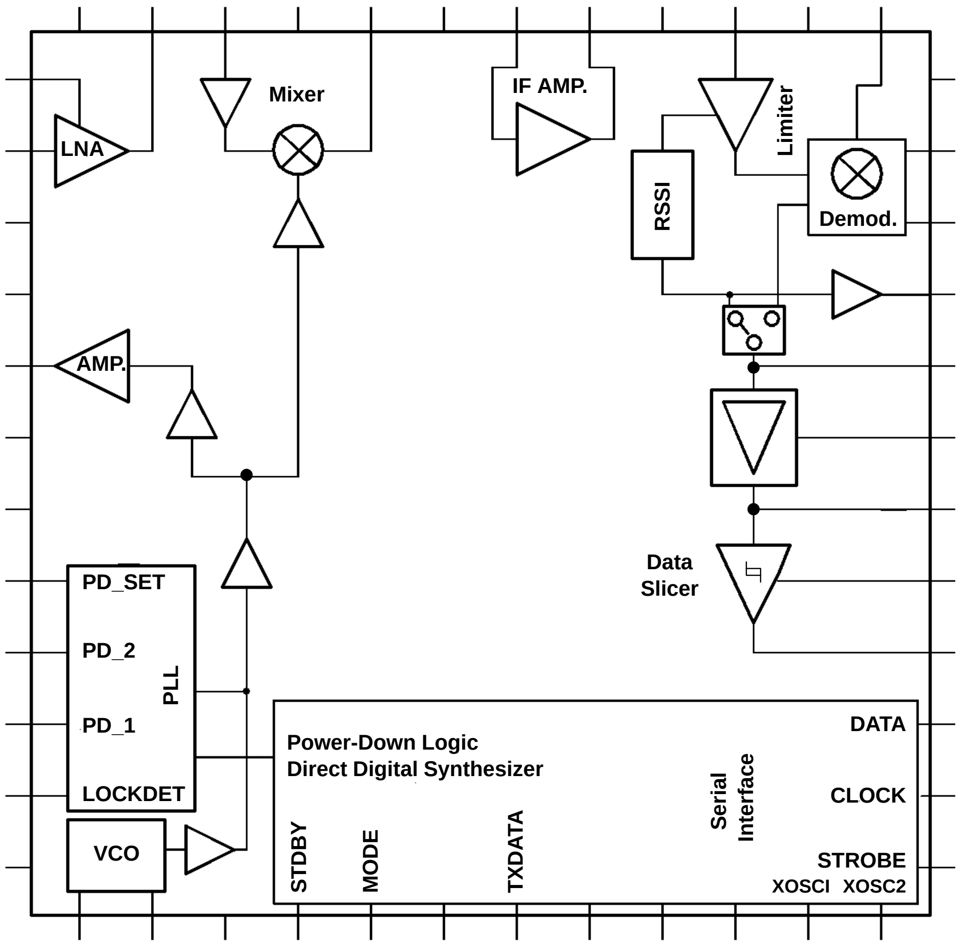


Figure 2. TRF6900 Functional Block Diagram

Overall, the TRF6900 combines a low-noise amplifier, RF Mixer, IF amplifier, limiter, fast RSSI, FM/FSK demodulator, low-pass filter amplifier, data slicer, fully programmable DDS, PLL, VCO, and power amplifier. These functions are briefly described in the following sections. For a detailed description, please review the TRF6900 and MSP430x112 product datasheets.

Ample TRF6900 terminals are provided as GND. These GND terminals are used to provide a high degree of signal grounding and to minimize crosstalk.

4.1 Serial Control Interface

All TRF6900 functional blocks can be individually powered up or down via the serial interface. The interface register can be programmed via a 3-wire serial data port using the CLOCK, DATA, and STROBE lines.

One 24-bit word is clocked into a temporary holding register with the most significant bit clocked first. The operation registers are loaded with the new data residing in the temporary registers, by the rising edge of the STROBE line.

Table 1 lists the format of the control words. For a detailed description of all serial registers and a timing diagram, please review the enclosed TRF6900 data sheet.

A–Word (Programming of DDS_0)

MSB … LSB

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	DDS Divder Ratio for Mode 0 (DD_1 [21:0])																					
Addr.																							

DDS Divder Ratio for Mode (DD_1 [21:0])

B–Word (Programming of DDS_1)

MSB … LSB

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	DDS Divder Ratio for Mode 1 (DD_1 [21:0])																					
Addr.																							

C–Word (Enable Register for PLL, Data Slicer and Mode 1 Settings)

MSB … LSB

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	PLL						X	X	Mode 1 Register [21:0]												
			APLL		NPLL		MM	SLCTL			PLL	VCO	PA		SCL	LPF	SW	RSSI	LIM	IF	MIX	LNAM	
Addr.			A2	A1	A0								P1	P0								L1	L0

D–Word (Enable Register for Modulation and Mode 0 Settings)

MSB … LSB

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	PLL						X	X	Mode 0 Register [21:0]												
			DEV								PLL	VCO	PA		SCL	LPF	SW	RSSI	LIM	IF	MIX	LNAM	
Addr.			DV7...							...DV0			P1	P0								L1	L0

Table 1. Serial Control Word Format

4.2 Low-Noise Amplifier

The low-noise amplifier (LNA) receives the incoming, modulated signal and boosts the level. Two operation modes, normal and low-gain mode, can be selected. The normal mode is selected when maximum sensitivity at low input levels is required. If high RF input levels are applied to the TRF6900, the LNA should be operated in the low-gain mode. Control is accomplished by using the LNA mode (LNAM) bits of the seriel control word.

A solder bridge (SW1) can be used to route the LNA output to the SMA connector J3 for evaluation of the LNA, or to the mixer input for cascaded evaluation.

4.3 Mixer

The mixer utilizes the on-chip synthesizer/VCO using low-side frequency injection to translate the received signal to the intermediate frequency (IF). The mixer’s output is a single-ended output with an impedance of approximately 330 Ω. On the EVM board, the output of the mixer is directly connected to a conventional 10.7 MHz ceramic filter without additional matching.

For evaluation, SW1 and SW2 can be used to connect the mixer to the SMA connectors J3 and J4. The matching network of L5, C12 is designed to transform 330 Ω into 50 Ω at 10.7 MHz. The matching network losses should be considered during evaluation.

4.4 IF Amplifier

The IF amplifier typically provides 7 dB of gain to compensate for the losses caused by the 10.7 MHz ceramic filter. The input and output of the IF amplifier are matched to 330 Ω, permitting a direct connection to a 10.7 MHz ceramic filter. For evaluation, SW2 and SW3 can be used to connect the amplifier to the SMA connectors J4 and J5. The matching network of L5, C12 and L6, C14 is designed to transform 330 Ω into 50 Ω at 10.7 MHz. The matching network losses should be considered during evaluation.

In order to provide for cascaded operation of the LNA, mixer, and IF amplifier, it is possible to configure a complete receiver chain by soldering SW1, SW2, and SW3 accordingly.

4.5 Second IF Amplifier/Limiter

This block provides an additional 80 dB of gain. At the 330 Ω input, a minimum signal level of approximately 32 µV is required to generate a limited signal at the limiter output. The limiter output is directly fed to the FM/FSK demodulator.

4.6 Radio Strength Signal Indicator

The receive strength signal indicator (RSSI) provides a voltage at terminal 33 that is proportional to the limited RF input level. Due to the fast response time, the RSSI can be used as an on/off keying (OOK) demodulator.

During learn mode (see Data Slicer section), an auto-zero loop is activated and corrects the dc offset for a proper 0 or 1 decision in the following data slicer. The time constant of the regulation loop is determined by C20 = 12 nF and is set on the EVM to approximately 260 µs. This requires that the duty cycle of the baseband signal be approximately 50% (bi-phase code). If the duty cycle is not 50% (as in NRZ codes), then a learning sequence is needed to properly utilize the implemented offset regulation loop. After a constant-dc learning or training sequence, the status of the data slicer can be changed from learning to hold mode and a non constant-dc data signal (NRZ code) can be used. Depending on parasitic effects, the external sample and hold capacitor (connected to terminal 29) will be discharged over time and must be periodically recharged to guarantee proper 0 or 1 decisions when using NRZ codes.

4.7 FM/FSK Demodulator

The demodulator is intended for use with linear (FM) and digital (FSK) frequency modulation. Demodulation of FSK or FM is accomplished by using an internal quadrature demodulator. The external LC tank circuit frequency is set to 10.7 MHz with a bandwidth of approximately 300 kHz. Due to an inductor (which is internal to the TRF6900) that is in parallel to the external tank circuit, no additional adjustments are required if the frequency tolerance of the external components is better than 5%.

4.8 Data Switch

The device incorporates a data switch to select the input signal for the post detection amplifier. Dependent on the settings in the enable registers (C-Word, D-Word) the user can select between OOK or FSK baseband processing.

4.9 Low-Pass Filter Amplifier

The filter amplifier is configured to operate as a second-order low-pass filter for post detection. The low-pass filter corner frequency on the EVM is set to approximately 180 kHz.

A solder bridge (SW4) can be used to route the input or output of the post detection amplifier to the SMA connector J6 for evaluation.

4.10 Reference Oscillator

The reference oscillator provides the DDS system clock. The EVM uses an 18 MHz clock to generate the PLL reference input signal. This value is the default setting for the DDS reference clock in the TRF6900 evaluation software (programming tool).

4.11 VCO

The external VCO tank circuit is designed to operate between 850 MHz and 890 MHz using the single SMV1233-011 varactor diode. The Q-factor of the VCO tank circuit is in the range of 50 to guarantee proper oscillation.

4.12 Phase Detector and Charge Pumps

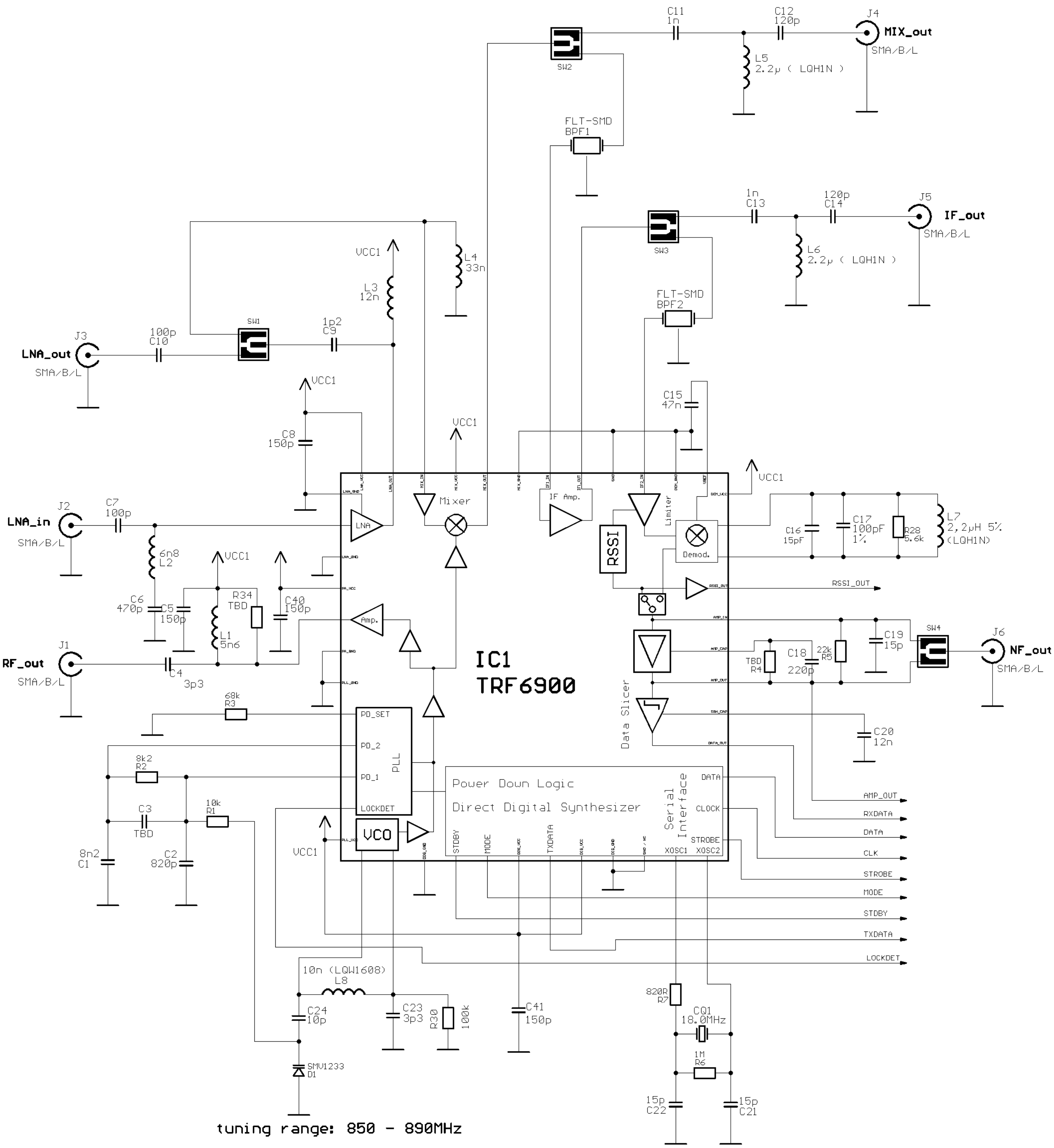
The device contains two charge pumps: one for coarse tuning (PD_2) and one for fine tuning (PD_1). The output current is determined by R3 = 68 kΩ.

4.13 Power Amplifier

The power amplifier (PA) can be programmed with two bits to operate on three different power levels. Several control loops are implemented internal to the TRF6900 to set the output power and to minimize the sensitivity of the power amplifier to temperature, load impedance, and power supply variations. The output stage of the PA operates in class C and enables simple impedance matching. On the EVM, the PA is matched to 50 Ω to ease the evaluation.

5 Evaluation Board Rev B

5.1 Schematic



TBD parts not populated

Figure 3. Schematic TRF6900/MSP430 EVM-TRF6900 (Rev B)

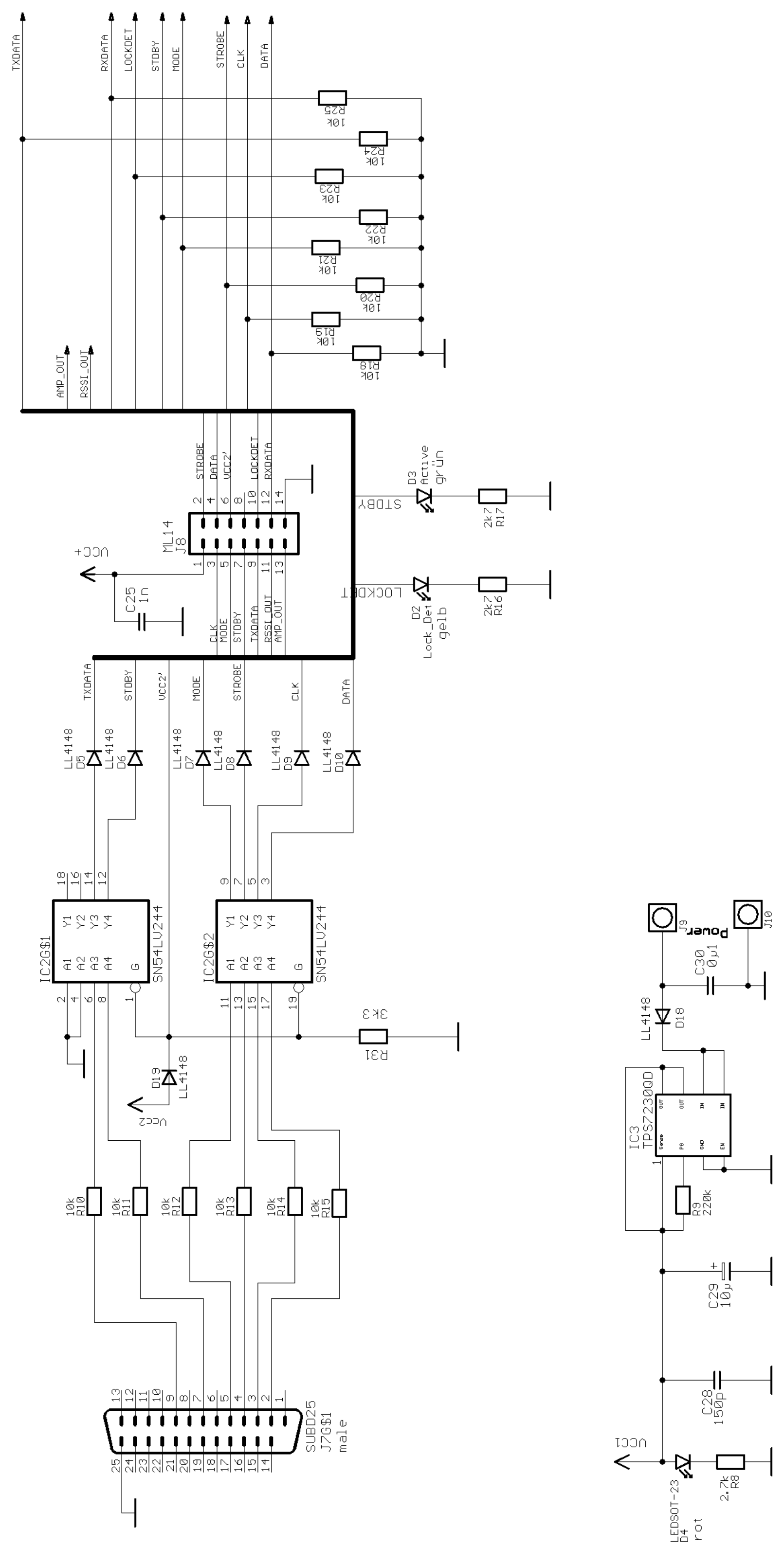


Figure 4. Schematic TRF6900/MSP430 EVM-Parallel Port (Rev B)

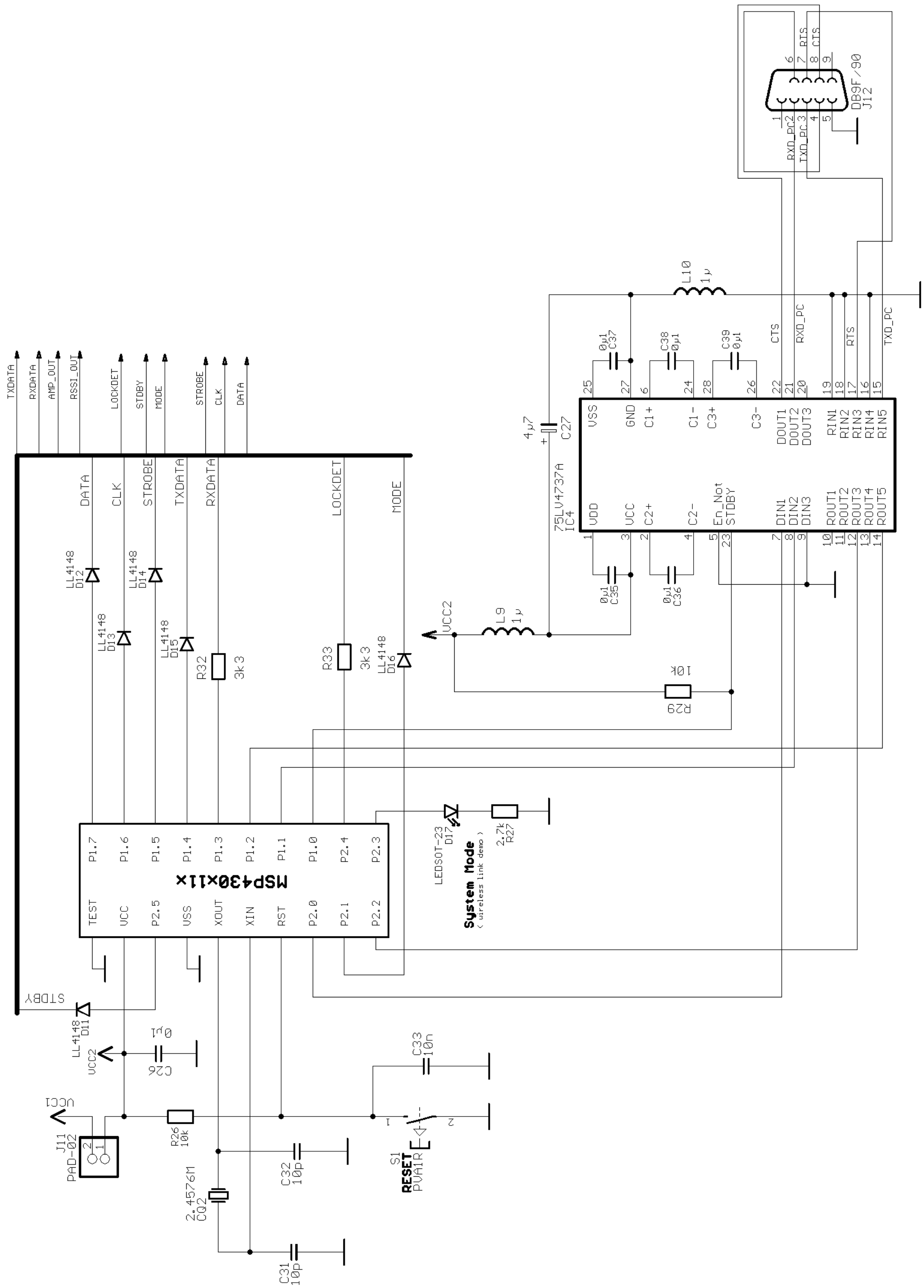


Figure 5. Schematic TRF6900/MSP430 EVM-MSP430 (Rev B)

6 Component Summary

Table 2. Parts List

POSITION	VALUE	PACKAGE	COMMENT
BPF1	SFECV10.7MJ-Z	FLT-SMD	3 dB BW 150 kHz, Murata
BPF2	SFECV10.7MJ-Z	FLT-SMD	3 dB BW 150 kHz, Murata
C1	8n2	0603	
C2	820p	0603	
C3	optional	0603	Not populated
C4	3p3	0603	
C5	150p	0603	
C6	470p	0603	
C7	100p	0603	
C8	150p	0603	
C9	1p2	0603	
C10	100p	0603	
C11	1n	0603	
C12	12p	0603	
C13	1n	0603	
C14	120p	0603	
C15	47n	0603	
C16	15p	0603	Tolerance 5%
C17	100 pF	0603	Tolerance 1%
C18	220p	0603	
C19	15p	0603	
C20	12n	0603	
C21	15p	0603	
C22	15p	0603	
C23	3p3	0603	
C24	10p	0603	
C25	1n	0603	
C26	0 µ1	0805	
C27	4 µ7	TBD	
C28	150p	0603	
C29	10 µ	1812	
C30	0µ1	0805	
C31	10p	0603	
C32	10p	0603	
C33	10n	0603	
C35	0µ1	0805	
C36	0µ1	0805	
C37	0µ1	0805	
C38	0µ1	0805	
C39	0µ1	0805	
C40	150p	0603	
C41	150p	0603	

Table 2. Parts List (Continued)

POSITION	VALUE	PACKAGE	COMMENT
CQ1	93M180–20	SMD-93SMX	18 MHz, ±50 ppm (optional ±20 ppm)
CQ2	2.4576 MHz	HC-49/U-SMD	2.4576 MHz, ±20 ppm @ 25°C
D1	SMV1233–11	SOD-323	Alpha Industries Inc.
D2	LED/yellow	SOT-23	Lock_Det, SMD type
D3	LED/green	SOT-23	Active, SMD type
D4	LED/red	SOT-23	Vcc, SMD type
D5	LL4148	MINIMELF	
D6	LL4148	MINIMELF	
D7	LL4148	MINIMELF	
D8	LL4148	MINIMELF	
D9	LL4148	MINIMELF	
D10	LL4148	MINIMELF	
D11	LL4148	MINIMELF	
D12	LL4148	MINIMELF	
D13	LL4148	MINIMELF	
D14	LL4148	MINIMELF	
D15	LL4148	MINIMELF	
D16	LL4148	MINIMELF	
D17	LED/red	SOT-23	Sys_Mode, SMD type
D18	LL4148	MINIMELF	
D19	LL4148	MINIMELF	
IC1	TRF6900	QFP48	Texas Instruments
IC2	SN54LV244APW	TSSOP20	Texas Instruments
IC3	TPS7230QD	SO-8	Texas Instruments
IC4	75LV4737ADB	SSOP-28	Texas Instruments
IC5	MSP430P112IDW	SOIC-20L	Texas Instruments
J1	SMA/B/L	SMA/B/L	
J2	SMA/B/L	SMA/B/L	
J3	SMA/B/L	SMA/B/L	
J4	SMA/B/L	SMA/B/L	
J5	SMA/B/L	SMA/B/L	
J6	SMA/B/L	SMA/B/L	
J7	SUBD25	SUBD25	25-pin male connector
J8	ML14	ML-14	
J9	01CON	1CON	Bolted connection
J10	01CON	1CON	Bolted connection
J11	PAD-02	PAD-02	Jumper (Sys_Mode)
J12	DB9F/90		Female connector for RS232
L1	5n6	0603	LQW1608/Murata, TFL0816/SUSUMU
L2	6n8	0603	LQW1608/Murata, TFL0816/SUSUMU
L3	12n	0603	LQW1608/Murata, TFL0816/SUSUMU
L4	33n	0603	LQW1608/Murata, TFL0816/SUSUMU
L5	2µ2	1206	LQH1N/Murata, ±10%
L6	2µ2	1206	LQH1N/Murata, ±10%

Table 2. Parts List (Continued)

POSITION	VALUE	PACKAGE	COMMENT
L7	2µ2	1206	LQH1N2R2J04/Murata, ±5%
L8	10n	0603	LQW1608/Murata
L9	1µ0	TBD	Tolerance ±10%
L10	1µ0	TBD	Tolerance ±10%
R1	10 k	0603	
R2	8k2	0603	
R3	68k	0603	
R4	optional	0603	Not populated
R5	22k	0603	
R6	1M	0603	
R7	820R	0603	
R8	2k7	0603	
R9	220k	0603	
R10	10k	0603	
R11	10k	0603	
R12	10k	0603	
R13	10k	0603	
R14	10k	0603	
R15	10k	0603	
R16	2k7	0603	
R17	2k7	0603	
R18	10k	0603	
R19	10k	0603	
R20	10k	0603	
R21	10k	0603	
R22	10k	0603	
R23	10k	0603	
R24	10k	0603	
R25	10k	0603	
R26	10k	0603	
R27	2k7	0603	
R28	5k6	0603	
R29	10k	0603	
R30	100k	0603	
R31	3k3	0603	
R32	3k3	0603	
R33	3k3	0603	
R34	TBD	0603	
S1	Reset	PVA1R	

Table 3. Semiconductors

QUANTITY	VALUE	PACKAGE	PARTS
15	LL4148	MINIMELF	D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, D16, D17, D18, D19
1	SMV1233-11	SOD-323	D1
1	LED/yellow	SOT-23	D2
1	LED/green	SOT-23	D3
2	LED/red	SOT-23	D4, D17
1	TRF6900	QFP48	IC1
1	SN54LV244A	TSSOP20	IC2
1	TPS7230QD	SO-8	IC3
1	75LV4737ADB	SSOP28	IC4
1	MSP430P112IDW	SOIC-20L	IC5

Table 4. Capacitors

QUANTITY	VALUE	PACKAGE	PARTS
1	TBD	0603	C3
1	1p2	0603	C9
2	3p3	0603	C23, C4
3	10p	0603	C24, C31, C32
4	15p	0603	C16, C19, C21, C22
3	100p	0603	C7, C10, C17
2	120p	0603	C12, C14
5	150p	0603	C5, C8, C28, C40, C41
1	220p	0603	C18
1	470p	0603	C6
1	820p	0603	C2
3	1n	0603	C11, C13, C25
1	8n2	0603	C1
1	10n	0603	C33
1	12n	0603	C20
1	47n	0603	C15
7	0µ1	0805	C26, C30, C35, C36, C37, C38, C39
1	4µ7	TBD	C27
1	10µ	1812	C29

Table 5. Inductors

QUANTITY	VALUE	PACKAGE	PARTS
1	6n8	0603	L2
1	10n	0603	L8
1	12n	0603	L3
1	33n	0603	L4
2	1µ0	TBD	L9, L10
1	2µ2 5%	1206	L7
2	2µ2 10%	1206	L5, L6
1	5n6	0603	L1

Table 6. Resistors

QUANTITY	VALUE	PACKAGE	PARTS
1	820R	0603	R7
4	2k7	0603	R8, R16, R17, R27
3	3k3	0603	R31, R32, R33
1	5.6k	0603	R28
1	8k2	0603	R2
18	10k	0603	R1, R10, R11, R12, R13, R14, R15, R18, R19, R20, R21, R22, R23, R24, R25, R26, R29, R31
1	22k	0603	R5
1	68k	0603	R3
1	100k	0603	R30
1	220k	0603	R9
1	1M	0603	R6

Table 7. Crystals

QUANTITY	VALUE	PACKAGE	PARTS
1	18.0 MHz	SMD	CQ1
1	2.4576M	SMD	CQ2

Table 8. Connectors

QUANTITY	VALUE	PACKAGE	PARTS
1	DB9F/90	female	J12
1	ML14	ML-14	J8
1	PAD-02	PAD-02	J11
6	SMA/B/L	SMA/B/L	J1, J2, J3, J4, J5, J6
2	01CON	1CON	J9, J10
1	SUBD25	male	J7

Table 9. Switches

QUANTITY	VALUE	PACKAGE	PARTS
1	PVA1R	Reset	S1

Table 10. Filters

QUANTITY	VALUE	PACKAGE	PARTS
2	FLT-SMD	FLT-SMD	BPF1, BPF2

Many of the components used on the EVM aid in taking measurements, emulate a serial data interface, and inject signals in a 50-Ω environment. In addition, an MSP430x112 is included on the EVM board to demonstrate a serial RF link. In actual use, the component count would be greatly reduced.

6.1 PCB Layout

The evaluation board (EVM) is comprised of a four-layer printed-circuit board (PCB), a TRF6900 device, several SMA connectors, and all necessary peripheral discrete components to evaluate the transceiver.

The EVM also includes a programmed MSP430x112 including all external components to set up an RF link in the new European 868 MHz to 870 MHz band.

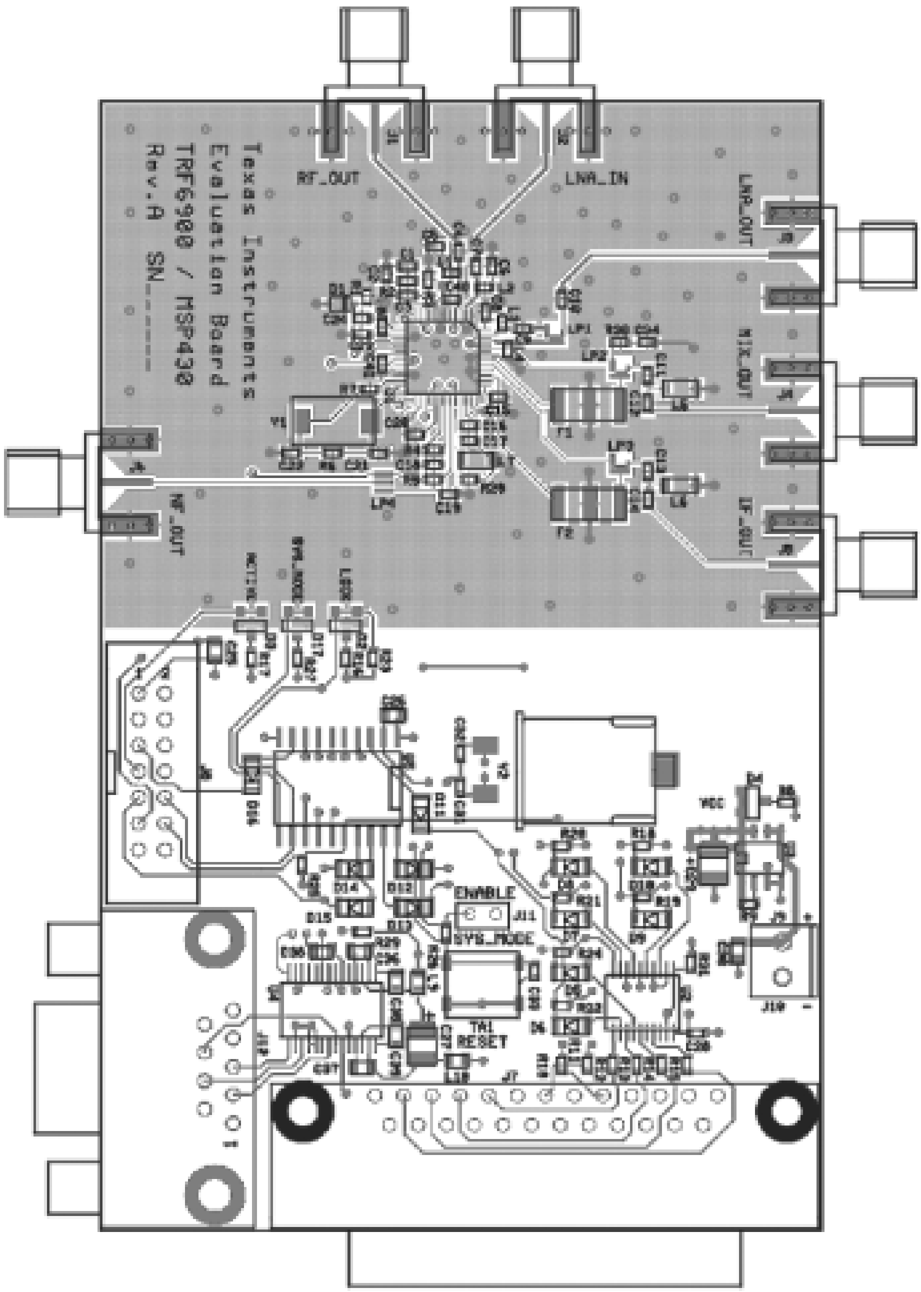


Figure 6. EVM PCB Layout

6.2 Power Supply

External power should be connected to the evaluation board at J9 (POWER) and J10 (GND). It is recommended that the user set the power supply between 3.2 VDC and 9 VDC.

The onboard low-dropout voltage regulator, the TPS7230, is a 3-V regulator with a drop-out voltage of $<$150mV. A 10 µF capacitor, located close by, is used to reduce ripple and enhance noise rejection in the regulator.

6.3 Serial Interface

A DB25 connector, J7, is provided for connection to a standard PC parallel port using a 25-conductor cable. The PC parallel port is used to emulate a synchronous serial data interface consisting of CLOCK, DATA, and STROBE. The STDBY, MODE, and TXDATA lines can be controlled by the emulated microprocessor signal from the PC parallel port—see the section entitled *TRF6900 Programming Tool Software*.

All six interface signals from the PC parallel port are fed through the level converter LV244A to the TRF6900. In this manner, the TRF6900 device may be operated at any supply voltage that is different from the standard 5-VDC voltage level of the PC parallel port.

The TRF6900 is specified to operate between 2.2 VDC and 3.6 VDC.

7 TRF6900 Programming Tool Software

A Windows-based software utility to program the TRF6900 via the parallel port of a PC is supplied with the evaluation board.

The software is located on the disk labeled TRF6900 programming tool.

The software is intended for use with Windows 95 or Windows 98. No special memory is required to use the software. The resolution of the video card should be equal to or higher than 800 x 600 pixels. To install the programming software on your PC, perform the following tasks:

- Start Windows
- Insert disk labeled TRF6900 Programming Tool into drive A
- From Program Manager, select File menu and choose RUN
- Type A:\setup and press Enter
- Follow the displayed instructions.

The installation shield guides you through the installation and copies all required files onto your system hard drive.

- You can start the program by executing the TRF6900.EXE file.

Remove the system mode jumper J11 on the EVM, connect the parallel interface cable to the computer LPT port and the EVM. The EVM software allows you to select the correct LPT port. The default LPT port is LPT1. Port selection is found under the Options menu.

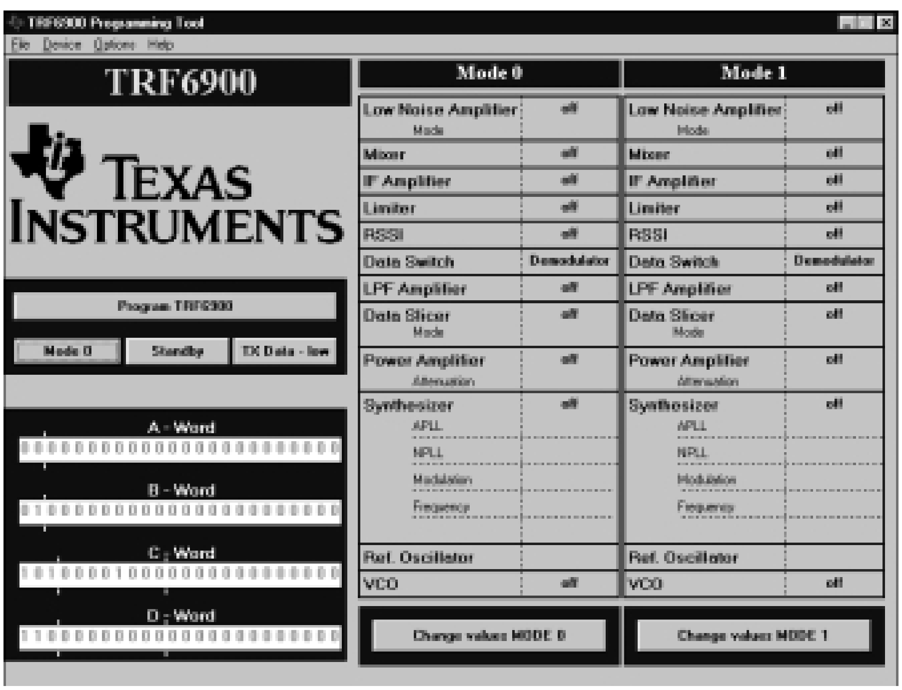


Figure 7. Visual Input Screen

7.1 Visual Input

When you start the programming tool, it comes up in the visual input mode. This mode can be used to calculate the settings to load the TRF6900 through the serial interface based on your inputs. On the right side, the calculated settings for the A-, B-, C-, and D-word appear. The current settings for Mode0 and Mode1 are shown on the left side. To change the Mode0/Mode1 settings press the Change values MODE0/Change values MODE1 button.

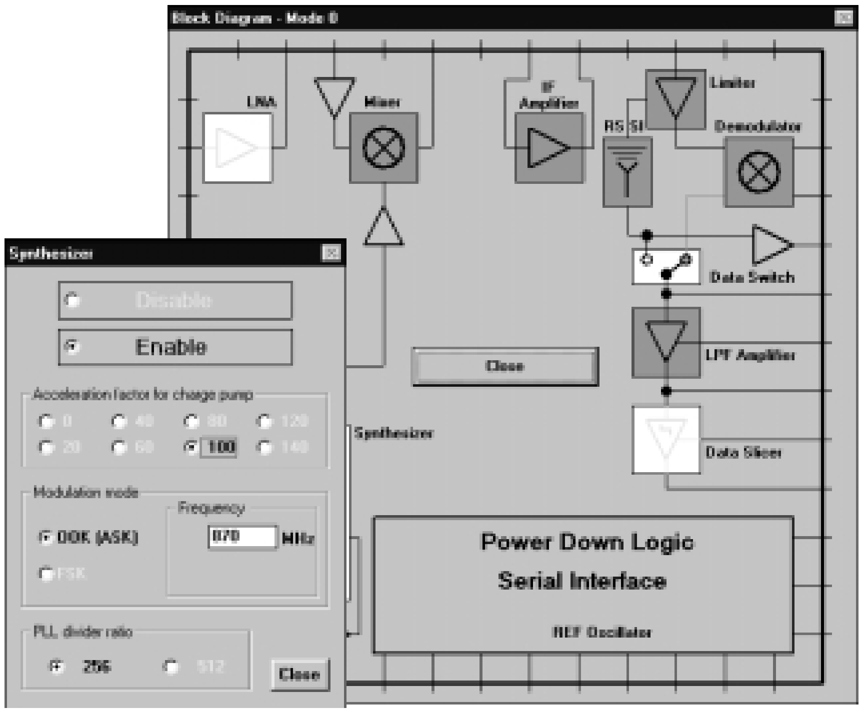


Figure 8. TRF6900 Block Diagram Included in the Programming Tool

A functional block diagram of the TRF6900 as shown in Figure 8 appears on the PC monitor. All blocks can be activated or deactivated individually by selecting the corresponding field on the block diagram. Available block selections are LNA, mixer, IF amplifier, limiter, RSSI, data switch, LPF, data slicer, VCO, synthesizer, and power amplifier.

To activate or deactivate a block, simply click on the desired field with the mouse—the color will change and indicate that the functional block was enabled (green) or disabled (white).

Some functional blocks require more detailed information (e.g., synthesizer, LNA, power amplifier, data slicer), and a new window to specify the additional parameters for the particular block will appear.

Once the functional blocks have been selected, select *Close* with the mouse to calculate the corresponding programming settings for the serial interface.

The settings, which are used to program the TRF6900, are now displayed in the visual input screen. To program the device, click on the *Program TRF6900* button and the data will be transferred to the TRF6900 via the parallel port of your PC. Starting with the A-Word, all words are programmed and the control lines are reset.

The *Standby*, *Mode 0* and *TX Data – low* buttons are used to control the corresponding TRF6900 terminals – please see the TRF6900 EVM schematic. Once you press the control field, the logical level toggles.

Using the file menu, the settings in the visual input can be saved or printed. The convert (bin) option can be used convert the settings of visual input screen to a file which can be post-edited at a later time by using the binary input screen.

7.2 Binary Input

Using the Option menu you can switch to the binary input screen to directly control the serial control word. A copy of the serial control word format, as shown in Figure 9, appears when you select Binary Input under the Option menu.

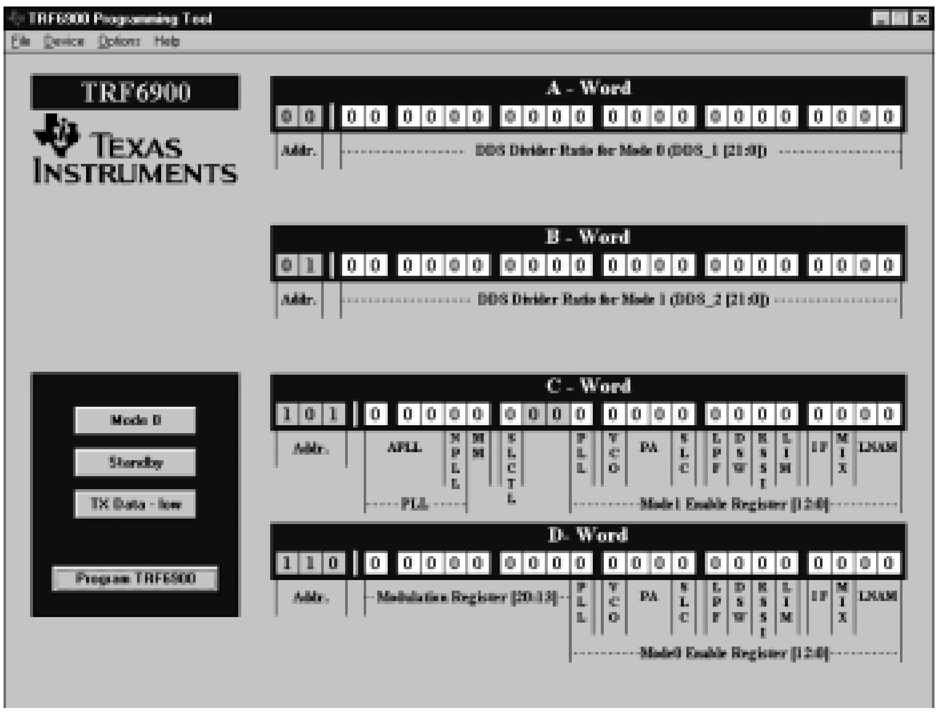


Figure 9. TRF6900 Serial Control Word Format

All bits, except the address bits, can be activated or deactivated by simply clicking—via the left mouse button—on the corresponding field. The content will change and the new value will be displayed.

As previously described, to program the device: click on the *Program TRF6900* button, and the data will be transferred. The *Standby*, *Mode 0* and *TX Data – low* buttons are used to control the TRF6900. Once you press the control field, the logical level toggles and the new status will be displayed. The file menu can be used to save and print the settings during the binary input.

8 TRF6900/MSP430 System Mode

Figure 10 shows an example setup of the EVM driven in system mode. The communication between the PC and the EVM runs with a baud rate of 19.200bit/s. The data transfer on the RF side is done at 38.400 baud (NRZ). The format of the RS232 communication protocol is transformed into a customized TRF6900-specific protocol as follows:

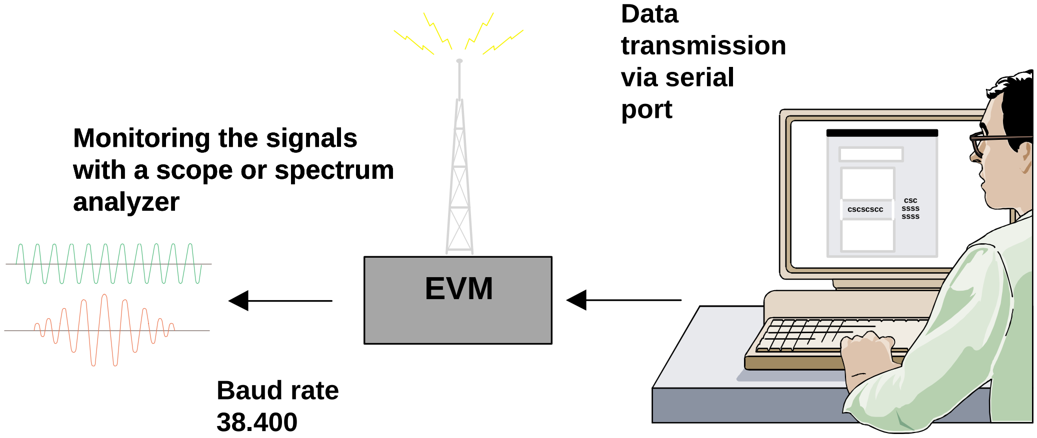


Figure 10. Setup of the EVM Running the TRF6900 Demo

Data format RS232:	Sequences of 40 bytes (= 20 characters) each byte: 1 start bit, 8 data bits, 1 stop bit, no parity
Data format RF:	Training (learning) sequence 4 ms with 26.04 µs pulses each, followed by 1 start bit (78.12µs) sequence of 40 bytes data, no stop bit
Data coding:	Nonreturn to zero (NRZ) after training sequence
Transmission technique:	Bidirectional, half-duplex

The following specification is used to set up the RF link in the 869MHz band:

Frequency of the output signal:	869,850 MHz
Modulation:	2-FSK, deviation ±30 kHz
IF frequency	10.7 MHz, 150 kHz bandwidth

8.1 Functionality in System Mode

The MSP430P112 device is programmed to emulate an application example. In this mode the user can investigate a simple, bidirectional serial RF data link. This mode is activated by the system mode jumper (J11). As soon as power is applied, the jumper J11 is set, and the reset button is pressed, the TRF6900 will be programmed via the MSP430 and the three LEDs (LOCK, SYS_MODE, ACTIVE) should light.

Using the TRF6900 demo software, the user can type in text in the TRF6900 demo window and send it to the EVM via RS232. The input window for the text is the Send window. As soon as the user presses the *Send* button, the data is sent. Every time the EVM receives a valid data package, the MSP430 terminates the reception of the data package and immediately switches off the red SYS_MODE LED for a few milliseconds. Hence, the user has visual feedback that the TRF6900/MSP430 EVM received a valid data package.

As soon the MSP430 has received the data package via RS232, the microprocessor jumps to the RF-send routine, switches the TRF6900 to send mode, and sends the received data out via RF as an FSK modulated signal. This RF signal can be sampled at the RF-Out SMA connector.

The received and sent data are displayed in the History window. The sent data is designated by 1>. The received data is designated by 2>. The transmitted data is stored in the History window. As soon the amount of data exceeds the range of the visible window, a scroll bar appears so that the user can scroll up and down.

8.2 TRF6900 System Mode Software

Windows-based software to run the application example (system mode) is included in the EVK.

The software can be installed from the two setup disks labeled MSP-EVK TRF6900 (TRF6900 demo).

The software is intended for use in a Windows environment, Windows95 or Windows98. No special memory is required to use the software. The resolution of the video card should be equal to or higher than 800 x 600 pixels.

8.3 Installing the TRF6900 System Mode Software

To install the programming software on your PC, perform the following tasks:

- Insert the setup disk 1.
- Start the setup program.
- Follow the displayed instructions.
- After finishing the installation, the software is ready to use.

8.4 Starting the EVM in System Mode

1. Set the system mode jumper on the evaluation board (EVM).
2. Connect the power supply to the TRF6900/MSP430 EVM (as a minimum, the red V_{CC} LED and SYS_MODE LED should light).
3. Connect the EVM via the serial cable to a free COM port on the PC.
4. Press the reset button (S1), the three LEDs (SYS_MODE, LOCK and ACTIVE) should light.

5. Starting the TRF6900 demo software; the window in Figure 11 comes up:

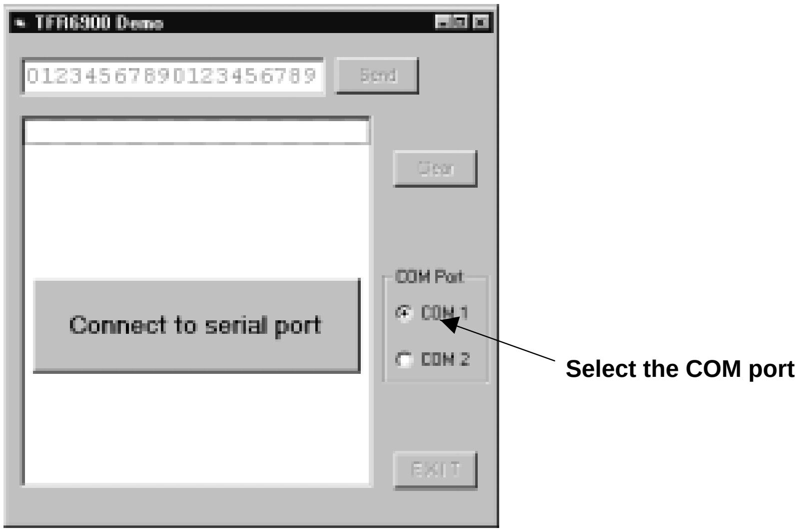


Figure 11. Initial State of the TRF6900 Demo

6. Select the COM port, which the EVM is connected to.

7. The EVM is now ready to send data. Type into the Send window and use the Send button to transmit the chat line. The communication flow will be displayed in the History window.

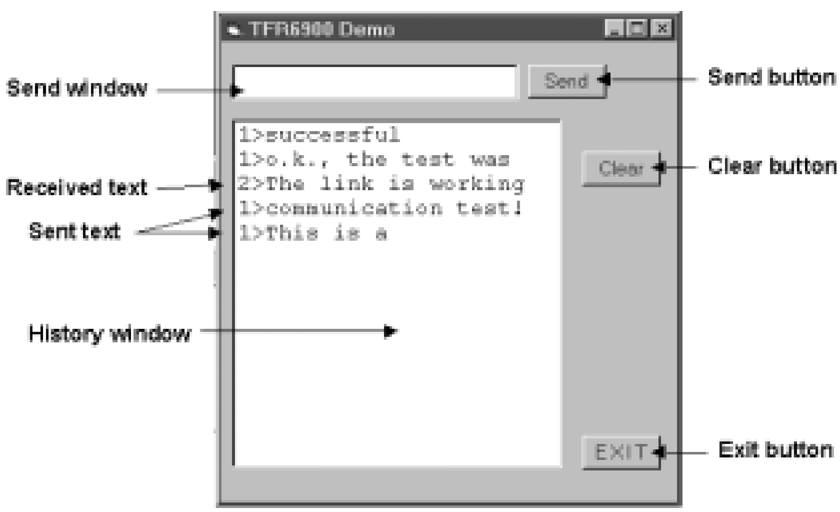


Figure 12. Running State of the TRF6900 Demo

8.5 Driving the EVM Board With an External Microcontroller

The EVM board is also prepared to monitor all digital lines of the TRF6900 to drive the TRF6900 by an external microcontroller. Table 11 details the pinout of the 14-pin header. The 14-pin header can be used to drive the RF-section on the EVK and to test a user-specific code running on an external microcontroller. The external MCU can directly connect to the 14-pin header.

Table 11. Terminal Functions of the 14-Pin Header

PIN NO.	CONNECTION	FUNCTION	PORT DIRECTION
1	V_{CC}	Positive power supply, 3 VDC	Out
2	STROBE	Strobe signal, serial programming of the TRF6900	In
3	CLK	Clock signal, serial programming of the TRF6900	In
4	DATA	Data signal, serial programming of the TRF6900	In
5	MODE	Switching between Mode 0 and Mode 1	In
6	NC	No connect	—
7	STDBY	Standby line of the TRF6900	In
8	NC	No connect	—
9	TXDATA	Transmission data line of the TRF6900	In
10	LOCKDET	Lock detect signal of the TRF6900	Out
11	RSSI_OUT	RSSI output signal of the TRF6900	Analog out
12	RXDATA	Data slicer output of the TRF6900	Out
13	AMP_OUT	Post detection amplifier output signal of the TRF6900	Analog out
14	GND	Ground of the power supply	In/Out

All relevant interface ports of the TRF6900 are available via this header. Note that the supply voltage of the TRF6900 in 3 V. Driving the parts with higher V_{CC} levels will destroy the device.

Please note that for this particular configuration, the MSP430 device mounted on the EVM board must be disabled. To disable the MSP430 mounted on the EVM, you must remove jumper J11. In this configuration, the parallel port driver LV244A is still active and could generate interferences if the DB25 connector, J7, for the parallel port is not properly terminated.

8.6 Evaluation Board Disclaimer

Please note that the evaluation boards that are enclosed with the kit are experimental printed-circuit boards and are therefore only intended for device evaluation.

We would like to draw your attention to the fact that these boards have been processed through one or more Texas Instruments external subcontractors, which have not been production qualified.

Device parameters measured, using these boards, are not representative of any final datasheet or of a final production version. Texas Instruments does not represent or assure that a final version will be made available after device evaluation.

The evaluation boards are supplied without warranty of any kind, expressed, implied or statutory, including but not limited to, any implied warranty of merchantability or fitness for a particular purpose.

Texas Instruments accepts no liability whatsoever arising as a result of the use of these boards.

9 References

1. *TRF6900 Single Chip Transceiver*, Literature number SLAS213
2. *TRF1020 GSM Receiver EVM*, Literature number SWRA018
3. *European Telecommunications Standard Institute Specification EN300 220-1*, V1.2 (1997–08)
4. *European Telecommunications Standard Institute Specification EN300 220-2*, V1.2 (1997–08)
5. *European Telecommunications Standard Institute Specification EN300 220-2*, V1.2 (1997–08)